

The Power Challenge - Intel's Holistic Approach to Power Management

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Abstract

Driven by Moore's Law, semiconductor manufacturers such as Intel are able to continually produce new innovative products that deliver increasing levels of performance and other user-valued capabilities. However, as more transistors are packed into a smaller area, power density increases, creating challenges for cooling and thermal management. Efficient power delivery and thermal management are critical as systems become smaller and more capable with every generation of new computing and communication products.

In 1983, the Intel® 286 microprocessor consisted of 134,000 transistors. Intel microprocessors today can contain over 1 Billion transistors (see Figure 1). Similarly, the computing power of the PC has increased by factors far exceeding 1,000X since the early 1980s. If the power consumed by an average PC had increased at the same rate, each one would require a 250-300 kilowatt (kW) power supply. Instead, for an average PC, the power consumed has stayed largely the same over the last 20 years despite dramatic improvements in PC performance and computing ability [1, 2].

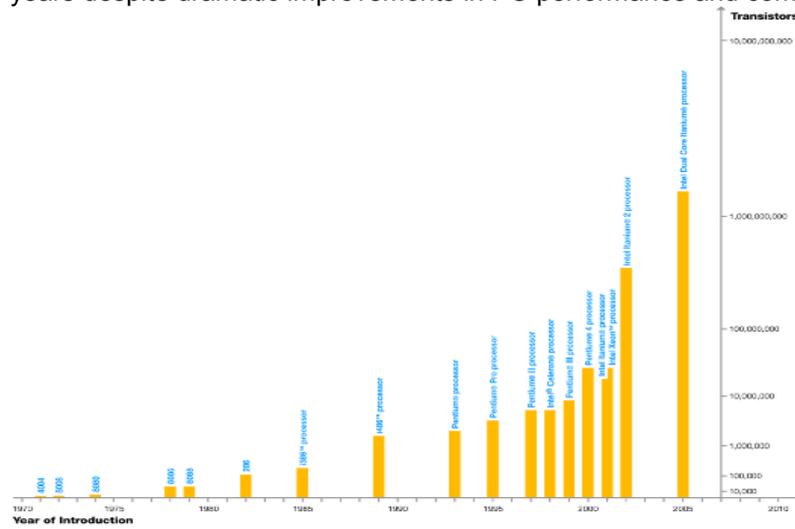


Figure 1: Growth in the number of transistors in an Intel CPU

The active power for a CMOS device is defined as: $P = CV^2f$, where P = active power needed for switching, C = total capacitance being switched, V = operating voltage and f = switching frequency. Although the switching frequency has increased dramatically over the past decade, Intel has focussed on driving both the voltage and capacitance down through improvements in manufacturing technologies. As a result, energy consumed per CMOS logic switching has decreased about 300X since the early 1990s [3].

Intel is a leader in developing innovative solutions to address and resolve power challenges. To be successful, Intel has taken a holistic approach toward power management by tackling the challenge at all levels: micro/macro architecture, silicon and circuit design & manufacturing, packaging, platform design, software optimization, and ecosystem enabling. Building on its past, but further emphasizing the future, in August 2005, Intel's CEO Paul Otellini announced a new product direction for the company that put even more emphasis on energy efficiency.

1. Intel Power Management achievements: Recent history

3.1 Mobile

In 2003, Intel released its Pentium® M processor which when combined with the Intel® 855 chipset family and the Intel® PRO/Wireless 2100 Network Connection made up the key building blocks of the Intel® Centrino™ mobile technology. Intel® Centrino™ mobile technology improves both performance and battery life over previous mobile processors. Energy efficiency has improved by over 30% using industry standard benchmarks [11].

In 2005, Intel released mobile processors with Enhanced Intel SpeedStep® technology and Intel® Mobile Voltage Positioning. Both technologies helped to minimize the power consumption of the mobile processor. Enhanced Intel SpeedStep® technology enables real-time dynamic switching of the voltage and frequency between two performance modes based on processor demand. Intel® Mobile Voltage Positioning (Intel® MVP IV) dynamically lowers voltage, based on processor activity. In partnership with the Mobile PC Extended Battery Life Working Group (www.eblwg.org), Intel led a successful effort to increase the energy efficiency of LCD's by about 40%. LCD screens are the largest source of power consumption in a notebook PC (~30-40% of the total power). This work successfully reduced the energy consumption of the screen from ~5 watts to 3 watts or less.

3.2 Desktop

When evaluating the total system power of a desktop PC, it can be seen that the processor consumes only about 10% of the total power. The video display devices and power supplies tend to dominate. If a CRT monitor is used, the monitor and power supply alone can account for up to 75% of the total desktop system power. If a LCD monitor is used, this value drops to about 50% of total system power [1].

Through research which started in 2000, Intel was able to show that the desktop PC power supply was a major source of energy inefficiencies for the system (some power supplies were as low as 50% efficient and most were designed to give optimum performance at full load). As a result of these findings Intel issued an update to its Power Supply Design Guidelines to include minimum energy efficiency targets for power supplies at 3 loadings – 20%, 50% and full load. As a result of these efforts, typical power supply efficiencies today are of the order of 80%.

Intel has a long history of actively working to improve the power management of PCs through work in industry groups to develop open industry specifications for power management. As an initial founder of Advanced Power Management (APM) and the follow-on Advanced Configuration and Power Interface (ACPI), Intel has helped develop and promote the use of sleep states to reduce overall system power consumption. In September 2004, ACPI version 3.0 was made available to the public. In 2005, a new feature was introduced into desktop (and server) products as a means of reducing platform idle power consumption. Enhanced autohalt (c1E) is a low power state entered into when the processor executes the HALT instruction. Since introduction, the autohalt feature has been continually optimized to enabling lower power states for the microprocessor.

There are many other examples of contributions from Intel to enable more power efficient desktop system designs such as: Intels integrated graphics chipset product line and the enabling of new form factor standards (actually Intels enabling of new form factors covers many market segments such as: mobile, ultramobile, workstation mobile, desktop, gaming machine, workstation, server, etc).

3.3 Servers

Servers present their own unique challenges for power management integration. Server systems can have multiple processors, significantly large memory, redundancies, multiple networking cards and hard drives. A server architecture, design and usage model is significantly different than a desktop or notebook PC. A server may be used locally or remotely with one or even millions of users.

Availability and response time to an uncertain frequency of requests for service is paramount. These requirements pose challenges for energy efficiency of servers and the facilities that host them.

In 2004, Intel launched its first server processor products with Enhanced Intel Speed Step® technology to support Demand Based Switching (DBS). DBS minimizes power consumption of the server system by dynamically changing the processor performance states. The performance states are changed based on demand for computing power and/or utilization. For systems using DBS, energy savings of up to 24% can be realized [12]. As illustrated in Figure 2, energy savings are greatest when processor utilization is less than 50%, decreasing as the processor approaches full utilization. Since most servers are utilized much less than 100% under typical operating conditions, DBS has the potential for significant energy savings.

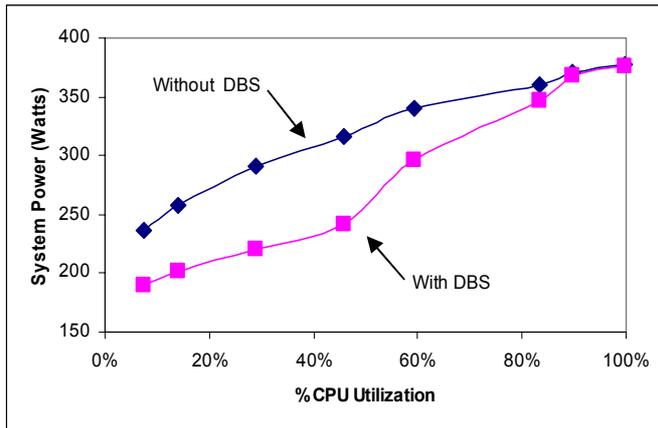


Figure 2: Effect of DBS on System Power Consumption

Intel introduced low voltage versions of its Intel® Xeon® processors in 2005. These processors can be used in server rack and blade designs where space is constrained and power-efficiency is a priority. These processors incorporate Demand Based Switching (DBS) technology. Technologies such as “autohalt (c1E)” (as mentioned under desktop PC above) and improved power supply efficiencies have also been introduced to server based products.

3.4 Silicon

In August 2005, Intel introduced its 65 nm manufacturing technology. 65 nm technologies allow printing of individual circuit lines on a semiconductor device at widths smaller than that of a virus. The gate within the transistor is even smaller, with a width of 35 nm and a thickness of 1.2 nm or 5 atomic layers [4]. At such small sizes, leaking current, which grows exponentially as the size of the transistor shrinks, becomes a problem. If steps are not taken to control it, leakage current can become a barrier to practical device operation [5].

3.4.1 Strained Silicon

Intel first introduced strained silicon into its 90 nm technology and is now used to manufacture many of Intel’s state of the art semiconductor products, such as the Intel® Core™ Duo processor. Strained silicon uses a region of silicon with built in stress, or strain, to increase the speed of the current flow across the transistor. By stressing or straining the silicon crystal lattice, electrons can flow with less resistance. Figure 3 illustrates this point. The result of such a technology is a 5-25X reduction in leakage current and 10-25% improvement in transistor current [5, 6, 7].

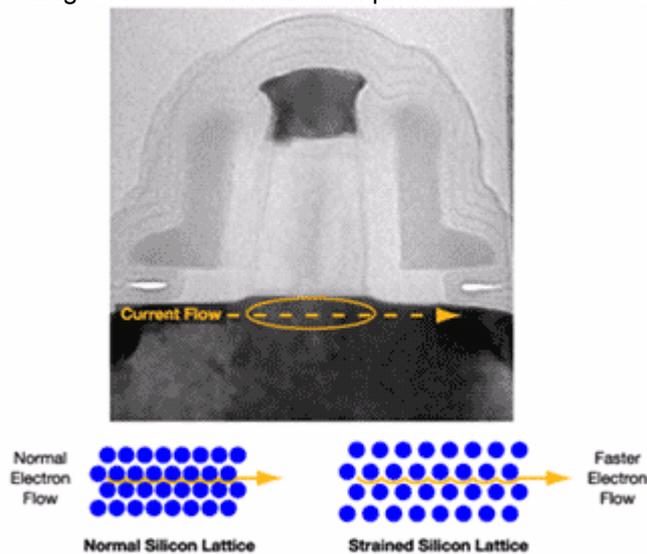


Figure 3: Illustration of Strained Silicon Benefits [8]

3.4.2 Sleep Transistors

Another method for reducing leakage current is to turn off, or put to sleep, the transistors of the silicon device which are idle or not actively in use. For example, Static Random Access Memory (SRAM) makes up a significant portion of Intel 65 nm microprocessors. SRAM is used to cache data and instructions. Sleep transistors can be used to shut off blocks of SRAM that are idle, saving energy by stopping the leakage current in these sections of the microprocessor [9].

3.4.3 High K Dielectric

In order to further reduce leakage at the gate, Intel has developed new thicker gate material termed “high-k dielectric.” The high-k material reduces leakage by 100 times over existing silicon dioxide materials [10]. Figure 4 is an image of both the traditional silicon dioxide gate and the new high-k gate material.

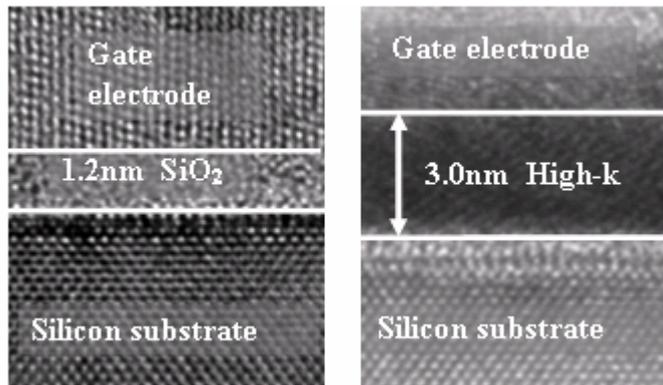


Figure 4: SEM image of existing SiO₂ gate material and new “high-k” gate material.

3.5 Power-Optimized microarchitecture

Intel continually strives to eliminate redundancy at the microarchitecture level by identifying frequent instruction sequences, extensively optimizing them, and storing them for later reuse. For example, Intel® NetBurst® microarchitecture has an advanced form of an instruction cache called the Execution Trace Cache, which stores already-decoded machine instructions or micro-ops for future reuse. Hyper-Threading Technology is another Intel microarchitecture that has been increasing performance without impacting the power envelope.

3.6 Offices and factories

In its offices and factories, Intel completed over 20 energy improvement projects in 2005. These projects resulted in savings of over 20 million kWhrs of electricity and nearly 2 million therms of natural gas. These results have been achieved through the use of improved controls, heat recovery, and other conservation techniques. The 2005 projects are part of an ongoing multi-year effort that has resulted in savings of over 200 million kWhrs of electricity and approximately 5 million therms of natural gas. Due to these projects, Intel’s energy used per unit of product manufactured has declined significantly over the last several years, well ahead of our publicly stated goal to reduce normalized consumption 4% per year. Intel has now begun working with the suppliers to drive improved efficiency in the manufacturing tools used in production. We believe progress in this area will complement the work begun on facility systems and continue to drive further improvements in the overall energy efficiency of the manufacturing process. More information is available at:

<http://www.intel.com/intel/other/ehs/perform.htm>

2. Intel Power Management achievements: Current achievements

In the microprocessor world, performance usually refers to the amount of time it takes to execute a given application or task or the ability to run multiple applications or tasks within a given period of time. However, true performance is a combination of both clock frequency (GHz) and Instructions Executed per Clock Cycle (IPC).

- Performance = Frequency x Instructions per Clock Cycle (IPC)

Therefore it is possible to increase performance by increasing clock frequency or instructions per clock cycle or both. Today, Intel is focusing on delivering optimal performance together with improved

energy efficiency, eg to take into account the amount of power the process will consume to generate the performance needed for a specific task.

As noted in the introduction, power consumption is related to the dynamic capacitance required to maintain IPC efficiency, times the square of the voltage that the transistors and I/O buffers are supplied with, times the frequency that the transistors and signals are switched at

- Power consumed = Capacitance x Voltage x Voltage x Frequency ($P = CV^2f$).

By taking into account both performance and power equations, designers can carefully balanced and therefore optimise performance and power efficiency.

3.1 Intel® Core™ microarchitecture: setting new standards for energy efficient performance

The move to multi-core processing has opened the door to many other micro-architectural innovations that further improve performance and energy efficiency. Intel Core microarchitecture is one such state-of-the-art micro-architectural update that has been designed to deliver increased performance combined with superior energy efficiency. The Intel Core microarchitecture is a new foundation for Intel architecture based desktop, mobile, and mainstream server multi-core processors and is expected to start shipping in Q3 2006.

3.1.1 Intel Wide Dynamic Execution

Intel Wide Dynamic Execution enables delivery of more instructions per clock cycle to improve execution time and energy efficiency. Every execution core is wider allowing each call to fetch, dispatch, execute and return up to four full instructions simultaneously (previous technologies could handle up to three instructions at a time).

3.1.2 Intel Intelligent Power Capability

Intel Intelligent Power Capability is a set of capabilities designed to reduce power consumption and design requirements. This feature manages the runtime power consumption of all the processor's execution cores. It includes an advanced power gating capability that allows logic control to turn on individual processor logic subsystems only if and when they are needed. Additionally, many buses and arrays are split so that data required in some modes of operation can be put in a low-power state when not needed. In the past implementing power gating has been challenging because of the power consumed in the powering down and ramping back up, as well as the need to maintain system responsiveness when returning to full power. Through Intel Intelligent Power Capability, Intel has been able to satisfy these concerns, ensuring both significant power savings without sacrificing responsiveness.

3.1.3 Intel® Advanced Smart Cache

The Intel® Advanced Smart Cache is a multi-core optimized cache that significantly reduces latency to frequently used data, thus improving performance and efficiency by increasing the probability that each execution core of a dual-core processor can access data from a higher-performance, more efficient cache subsystem.

3.1.4 Intel® Smart Memory Access

Intel® Smart Memory Access improves system performance by optimizing the use of the available data bandwidth from the memory subsystem and hiding the latency of memory accesses. Intel Smart Memory Access includes an important new capability called "memory disambiguation," which increases the efficiency of out-of-order processing by providing the execution cores with the built-in intelligence to speculatively load data for instructions that are about to execute before all previous store instructions are executed.

3.1.5 Intel® Advanced Digital Media Boost

Intel® Advanced Digital Media Boost is a feature that significantly improves performance when executing Streaming SIMD Extension (SSE/SSE2/SSE3) instructions. They accelerate a broad range of applications, including video, speech and image, photo processing, encryption, financial, engineering and scientific applications. The Intel Advanced Digital Media Boost feature enables these 128-bit instructions to be completely executed at a throughput rate of one per clock cycle, effectively doubling, on a per clock basis, the speed of execution for these instructions as compared to previous generations.

3.2 Platform-Scalable Architectures

The new Intel Core microarchitecture will provide a solid foundation for new server, desktop, and mobile platforms.

3.2.1 Server Platforms

Servers can deliver significantly greater compute performance and compute density. Intel is developing a DP Server processor optimized for dual-core based on the new, state of the art, Intel Core microarchitecture, codenamed Woodcrest. The Woodcrest processor is targeted for introduction in the third quarter of 2006 and will work within the Bensley server platform and the Glidewell workstation platform. The Bensley server platform and the Glidewell platform are targeted for introduction in the second quarter of 2006.

Intel will also deliver a quad-core (4 full execution cores) processor to the DP Server segment based upon this new microarchitecture, codenamed Clovertown. Clovertown is targeted for introduction in the first quarter of 2007, on the Bensley and Glidewell platforms.

For the MP server segment, Intel is also developing a MP Server processor optimized for quad-core based on this new microarchitecture, codenamed Tigerton. The Tigerton processor is targeted for introduction in 2007 and will work within the Caneland server platform.

3.2.2 Desktop Platform

Desktops can deliver greater compute performance as well as ultra-quiet, sleek and low-power designs.

Intel is developing a desktop-optimized, dual-core processor based on the new, state of the art, Intel Core microarchitecture, codenamed Conroe. The Conroe processor will work within the 2006 Digital Home platform codenamed Bridge Creek, and the 2006 Digital Office platform, codenamed Averill. Conroe is targeted for introduction in the third quarter of 2006.

Intel will also deliver a quad-core (4 full execution cores) processor to the high-end desktop based upon this new microarchitecture, codenamed Kentsfield. Kentsfield is targeted for introduction in the first quarter of 2007.

Mobile Platform

Laptop users can take advantage of the increased multi-core compute capability within the mobile form factors. Intel is developing a mobility-optimized, dual-core processor based on the new, state of the art, Intel Core microarchitecture, codenamed Merom. The Merom processor will work within the Intel® Centrino Duo® mobile technology-based platform and Merom is targeted for introduction to align with the 2006 holiday buying season.

3. Intel Power Management achievements: Looking further ahead

3.1 Low Power on Intel Architecture Project

In addition to technologies and products on the market today to improve energy efficiency, Intel is actively researching future technologies for possible future applications. For example, in the consumer and business marketplaces, smaller devices are proliferating. Smart phones, notebooks, and micro PCs are the leading edge of a wave of new devices designed for communication and entertainment. As part of Intel's vision of architectural innovation for convergence, the Intel Systems Technology Labs is working to accelerate these next-generation technologies and products.

The Low Power on Intel® Architecture (LPIA) project of STL focuses on researching and developing low-power technology building blocks for future Intel® architecture-based platforms. Key learning's from this research will lay the groundwork as Intel product development groups move toward low power on Intel architecture.

Using the research platform, the LPIA team is conducting research to better understand and reduce the thermal and physical demands of computing technology. A critical focus area is extending battery life for portable devices. In addition, the team is developing power management policies and metrics for future Intel architecture-based platforms.

Intel is also performing system-level profiling and benchmarking, spanning from the power source to power distribution and on to power consumers. Power-smart platforms will extend battery life and enhance user experiences by applying best-in-class power management technologies. Focused on system software policy management, the STL LPIA project is:

- Researching system-level power states and aggressive power-management policies
- Developing power metrics to calibrate power management in handheld devices
- Focusing future efforts on close cooperation with OS vendors for implementation

3.2 Tri-gate Transistors

Intel has also developed a novel three-dimensional design that helps make transistors that scale, perform, and address the current leakage problem seen in smaller dimension planar transistors. Tri-gate fully depleted substrate transistors have a raised plateau like gate structure with two vertical walls and a horizontal wall of gate electrode. This 3D structure improves the drive current while the depleted substrate reduces the leakage current when the transistor is in the off state. Reducing the leakage current in the off state translates to increased battery life in mobile devices.

Intel believes that these new discoveries can be integrated into an economical and high-volume manufacturing process to address the power and heat increases in increasingly smaller transistors.

3.3 Intel and QinetiQ Collaborate On Transistor Research

Researchers from the two companies have successfully built 'quantum well' transistors by integrating a new transistor material, pioneered by QinetiQ called indium antimonide (InSb). InSb is made up of elements found in the III and V columns of the periodic table. Transistors made of this material enable research devices to operate at very low voltages, while still rapidly switching and consuming little power. The research results obtained from the quantum well transistors research showed a 10x lower power consumption for the same performance, or conversely a 3x improvement in transistor performance for the same power consumption, as compared to today's traditional transistors.

4. Summary

Intels efforts in power management go back more than a decade (though this paper has focused on more recent activities). For example Intel was one of 13 companies to receive the EPA's first Energy Star Computer Awards back in 1994. Intel is an initial founder of Advanced Power Management (APM) and the follow-on Advanced Configuration and Power Interface (ACPI), Intel helped develop and promote the use of sleep states to reduce overall system power. In response to Energy Star's computer energy-efficiency specification, Intel developed in 2001 the new Instantly Available PC Power Management to improve sleep-state power management.

Intel today works closely with regulatory bodies such as the US EPA and EU/EC in driving Energy Star and other WW regulatory standards to improve computing platform energy efficiency. Today Intel is one of 20 companies working with the DOE and EPA to help define the new Energy Star specifications.

This paper has described a number of Intels recent past, present and future activities aimed at improving the energy efficiency of computer devices. These efforts can be summarised in the table below:

	Recent history	Today	Future
Servers	<ul style="list-style-type: none"> enhanced autohalt (c1E) Enhanced Intel Speed Step® technology Demand Based Switching low voltage versions of its Intel® Xeon® processors 	<ul style="list-style-type: none"> Intel® Core™ microarchitecture Intel Wide Dynamic Execution Intel Intelligent Power Capability Intel® Advanced Smart Cache Intel® Smart Memory Access Intel® Advanced Digital Media Boost 	<ul style="list-style-type: none"> Low Power on Intel® Architecture (LPIA) Tri-gate Transistors Intel and QinetiQ Collaborate On Transistor Research Ever smaller transistors (22nm) Etc
Desktop	<ul style="list-style-type: none"> Power Supply Design Guidelines Intel® Active Management Technology ACPI version 3.0 New form factors Integrated functionality enhanced autohalt (c1E) 		
Mobile	<ul style="list-style-type: none"> Intel® Centrino™ mobile technology Enhanced Intel SpeedStep® technology Intel® Mobile Voltage Positioning Mobile PC Extended Battery Life Working Group 		
Silicon	<ul style="list-style-type: none"> 65 nm manufacturing technology Strained Silicon Sleep Transistors High K Dielectric Intel® NetBurst® microarchitecture Hyper-Threading Technology 		

“Lead the industry in performance per watt across all market segments” is one of Intel’s strategies within its 2006 strategic objectives for 2006.

Intel observes that energy efficiency demand from users is most pronounced for notebook and server products. Notebooks, because of battery life demands and servers due to high end data center energy demands. Data centers increasingly want to add more computing performance. Doing so requires more energy efficient products in order to effectively cool and stay within the power budget of the datacenter.

Energy efficiency has not been a major market driver for desktop computers. However, factors such as acoustics and smaller form factors are beginning to drive this market need. Despite this, as can be seen in this paper, Intel is investing heavily in continually improving the energy efficiency of desktop products.

5. Conclusions

Moore’s Law will continue to drive advances in semiconductor manufacturing. Intel’s manufacturing process roadmap predicts the development and use of 22 nm technology by 2011. Such advancement will continue to make technical challenges such as leakage current even more pronounced. As a result, Intel has made power management a top priority in its technology roadmaps.

To be successful in addressing the power challenges of the PC, one must take a holistic approach toward power management, tackling the challenge at all levels: micro/macro architecture, silicon and circuit design & manufacturing, packaging, platform design, software optimization, and ecosystem enabling. Intel has taken such an approach and has made significant progress toward meeting these challenges.

- The need for raw computing performance has evolved into a drive for energy-efficient performance to meet people's expanding demands for more capabilities and higher performance – whether for smaller devices, longer battery life, or greater power savings. Intel is driving innovations in computing multi-core architectures to deliver new levels of performance, capabilities and energy efficiency.

- The Intel® Core™ microarchitecture, Intel's new foundation for delivering even greater energy efficient performance, is expected to deliver significant performance gains and power reductions in desktop (Conroe) and server (Woodcrest) processors and to extend the strong energy-efficient performance leadership of the Core Duo processor.
- Supporting the new multi-core architecture are Intel's unparalleled manufacturing capacity and the most energy-efficient performance CPU transistors in the world.
- Intel delivers energy-efficient performance advances across its architecture, silicon, platforms and software to help the industry's leading companies create new uses, build new markets, and meet the evolving needs of people and businesses worldwide.

Delivering energy-efficient performance requires a holistic effort across all common platform components – processors, chipsets, hard drives, power supplies, graphics cards, memory subsystems, displays, BIOS, software and more. Intel's manage these components as a collective system. This creates a platform whose components work together to deliver performance when required and to conserve resources when one or more individual resources are not needed. Building energy efficient products in energy efficient buildings is without question high on Intels agenda. Technology realities and market demand are two of the factors determining our strategic research agenda direction on energy efficiency.

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